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SFWB265JF



## Specifications and Applications Information

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### Smart Force™ Dual Lamp Inverter

The ERG SFW Series of DC to AC inverters is specifically designed for applications which require high efficiency, wide dimming and LCD brightness stability over a wide input voltage range.

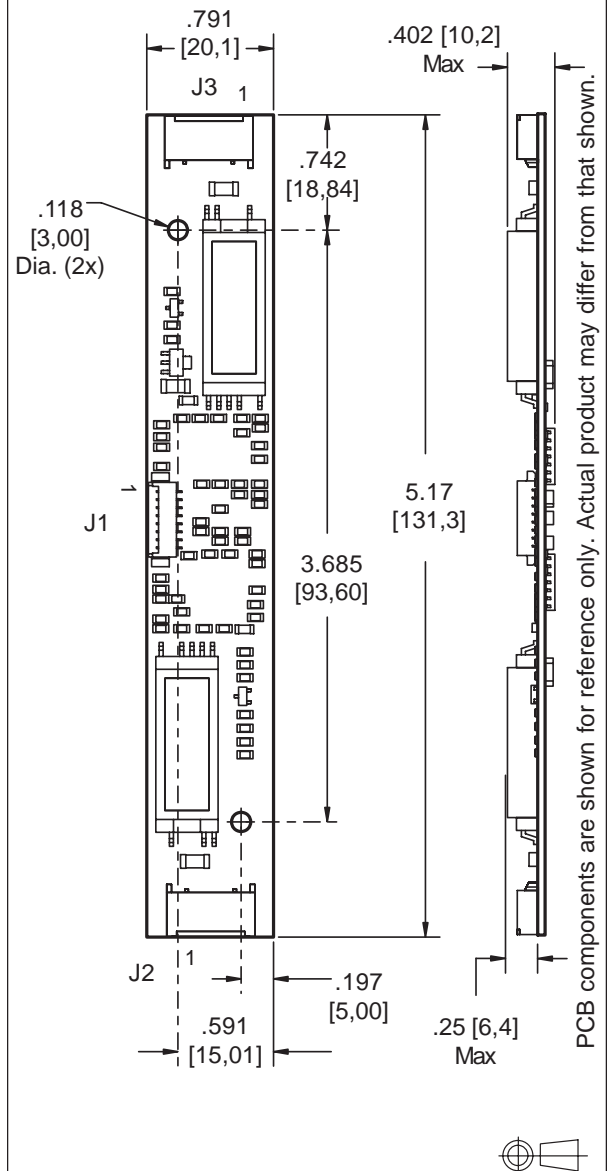
Designed, manufactured and supported within the USA, the SFW series features:

- ✓ Less than 10.3mm in Height
- ✓ Onboard regulation of lamp current
- ✓ High efficiency
- ✓ Open lamp detection
- ✓ Onboard analog dimming
- ✓ Support for a wide range of displays
- ✓ Low EMI emission

**\*\* Specific connection instructions and required power up sequence requirements are detailed on page 3.**



### Package Configuration



### Connectors

Input Connector	Output Connector
Molex 53261-0871	JST SM02(8.0)B-BHS-1-TB
J1-1 +Vin J1-2 +Vin J1-3 GND J1-4 GND J1-5 Enable J1-6 Control J1-7 N/C J1-8 GND	J2-1 ACout J2-2 ACreturn  J3-1 ACout J3-2 ACreturn



## Absolute Maximum Ratings

Rating	Symbol	Value	Units
Input Voltage Range	$V_{in}$	-0.3 to +25.0	Vdc
Enable	$V_{Enable}$	-0.3 to $V_{in}$	Vdc
Control	$V_{Control}$	-0.3 to +5.5	Vdc
Ambient Operating Temperature	$T_a$	-20 to +85	°C
Storage Temperature	$T_{stg}$	-40 to +85	°C

## Operating Characteristics

Unless otherwise noted  $V_{in} = 12.0$  Vdc,  $T_a = 25^\circ\text{C}$ , with a simulated load and unit has been running for 5 minutes.

Characteristic	Symbol	Min	Typ	Max	Units
Input Voltage <sup>(note 1)</sup>	$V_{in}$	+8.0	+12.0	+23.0	Vdc
Input Current <sup>(note 2)</sup>	$I_{in}$	-	0.89	1.00	Adc
Operating Frequency	$F_o$	-	56	-	kHz
Minimum Output Voltage <sup>(note 3)</sup>	$V_{out (min)}$	1500	-	-	Vrms
Efficiency <sup>(note 4)</sup>	<b>h</b>	-	82	-	%
Output Current (per lamp) <sup>(note 5)</sup>	$I_{out}$	-	6.5	-	mArms
Output Voltage <sup>(note 6)</sup>	$V_{out}$	-	-	720	Vrms
<b>Enable Pin</b>					
Turn-off Threshold	$V_{thoff}$	GND	-	0.5	Vdc
Turn-on Threshold	$V_{thon}$	2.4	-	$V_{in}$	Vdc

Specifications subject to change without notice.

- (Note 1)  $V_{in}$  is measured at the pcb connector.  
 (Note 2) Input current in excess of maximum may indicate a load/inverter mismatch condition, which can result in reduced reliability. Please contact ERG technical support.  
 (Note 3) Provided data is not tested but guaranteed by design.  
 (Note 4) 655 Vrms lamp voltage used in efficiency calculation.  
 (Note 5) The output current is measured from the AC return lead of the inverter using a Tektronix CT-2 AC current probe terminated into 50 ohms at the oscilloscope input.  
 (Note 6) Max allowable lamp voltage.



## Onboard Analog Dimming

Unless otherwise noted  $V_{in} = 12.0 \text{ Vdc}$ ,  $T_a = 25 \text{ }^\circ\text{C}$  and unit has been running for 5 minutes.

Characteristic	Symbol	Min	Typ	Max	Units
Minimum Brightness	$V_{\text{control}}$	-	5.0	-	V
Maximum Brightness	$V_{\text{control}}$	-	0.8	-	V

## Pin Descriptions

- Vin** Input voltage to the inverter.
- GND** Inverter ground.
- Control** Analog voltage input to the onboard dimming control. Graph 1 shows the relationship between  $V_{\text{control}}$  and relative display brightness.
- Enable** Inverter Enable.

## Application Information

The SFWB265JF inverter is designed to power two cold cathode fluorescent lamps from a wide input voltage source. Enabling the inverter is accomplished by applying a voltage greater than  $V_{\text{thon}}$  minimum to the Enable pin of the inverter.

An analog voltage is applied to the Control pin to change brightness. Figure 1 shows how to connect the inverter for analog dimming operation. Graph 1 shows the relationship of brightness to control voltage.

As with all inverters, it is important to take notice that the voltage present at the output pins is quite high and requires special care to be taken when integrating into the final application. The inverter should not be mounted closer than 0.180" (4.6mm) from any other conductive material. In general, the mounting hardware should be nonconductive. The exposed high voltage transformer, capacitor and connector leads are coated so as to provide reliable operation at altitudes up to 10,000 feet.

To improve the electrical efficiency of the overall application, the input harness cabling should be less than 12 inches (30 cm). The cable assembly between the inverter and the display is best kept below 4 inches (10 cm). If there are any questions or concerns, please feel free to contact ERG for exceptions or recommendations.

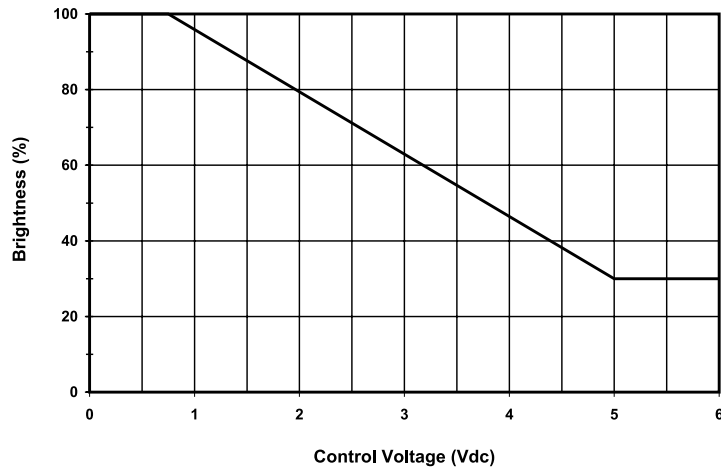
## REQUIRED POWER UP SEQUENCE

1. Set  $V_{in}$ , Enable and Control to 0(zero) Vdc.
2. Apply  $V_{in}$  power.
3. Apply Enable signal.
4. Apply and adjust control signal for desired brightness.

**Premature inverter shutdown may occur if the required power up sequence is not adhered to. No specific power down sequence is necessary.**

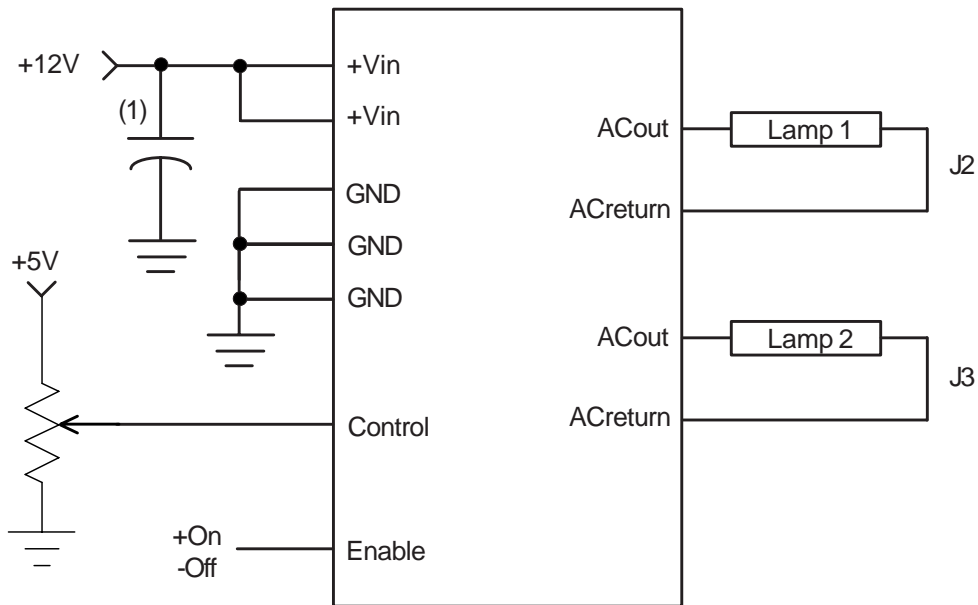


### Control Voltage vs. Brightness



### Graph 1

### Analog Dimming



### Figure 1

(1) Low ESR type input by-pass capacitor (22  $\mu$ F - 220  $\mu$ F) may be required to reduce reflected ripple, and to improve power supply transient response.



Endicott Research Group, Inc. (ERG) reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by ERG is believed to be accurate and reliable. However, no responsibility is assumed by ERG for its use.